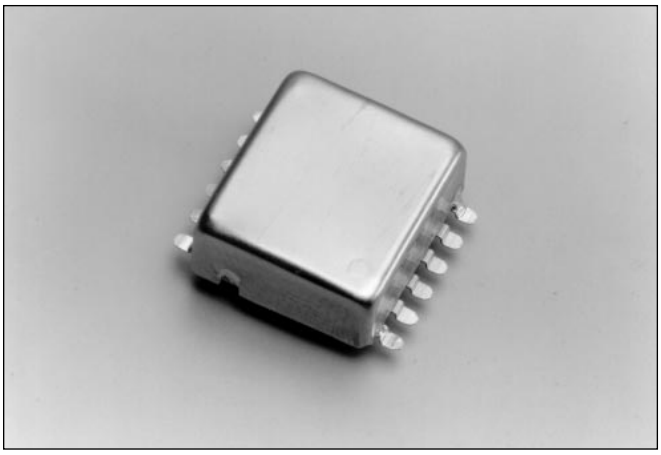
Surface Mount Frequency Synthesizer DATA 1005 - 1065 MHz

MLS9900-01035

V1.00

Features

- Miniature Size
- Surface Mount Package
- Electrically Shielded
- Low Phase Noise
- Integral Buffer Amplifier



Description

The MLS9900-01035 frequency synthesizer combines a phase locked loop circuit with a high performance buffered VCO in an RFI screened surface mount package. The synthesizer is optimised for mobile data service applications with 12.5 kHz or 25 kHz RF channel spacing. A +5V power supply and serial data input are required.

The surface mount package used provides for electrical shielding, ease of assembly and repeatable performance. M/A-COM's surface mount manufacturing techniques, automatic assembly and electrical testing ensure a high degree of electrical and mechanical repeatability at low cost and in high volume. Manufacturing is carried out in an ISO 9000 qualified facility.

Electrical Specifications[1], T_A = +25°C, V_{CC} = +5V (unless otherwise stated)

Parameter	Test Conditions	Units	Min.	Typ.	Max.
Frequency Range (Fout)		MHz	1005		1065
RF Output Power[2]	1005 - 1065 MHz	dBm	-2.0		+2.0
Supply Voltage (V_{CC1})		V	+4.75	+5.00	+5.25
Supply Current (I_{CC1})		mA			20
Supply Voltage (V_{CC2})		V	+4.75	+5.00	+5.25
Supply Current (I_{CC2})		mA			10
Reference Frequency (F_R)[3]	0.5 - 2.0 V pk - pk sine wave	MHz	1		20
Phase Noise[4]	SSB at 10 kHz offset from carrier	dBc/Hz		-100	-95
Residual Phase Noise	50 Hz to 100 kHz	Degrees		6.5	
Frequency Step Size (ΔF)		kHz		12.5	
Lock Up Time[5]	f_o ± 1 kHz band edge to edge	ms			40
Lock Up Time	between adjacent channels	ms			20
Harmonic Outputs		dBc		-20	-10
Spurious Outputs	f_o ± 12.5 kHz	dBc		-80	-75
Output Impedance		ohm		50	

1. All specifications apply with a 50 ohm load impedance.
2. Output power window includes unit to unit variation, temperature effects -30°C to +70°C and frequency flatness.
3. Reference frequency input impedance 10 kohm min.
4. For typical phase noise at other offsets see phase noise curve.
5. Integral lock detector, output high locked.

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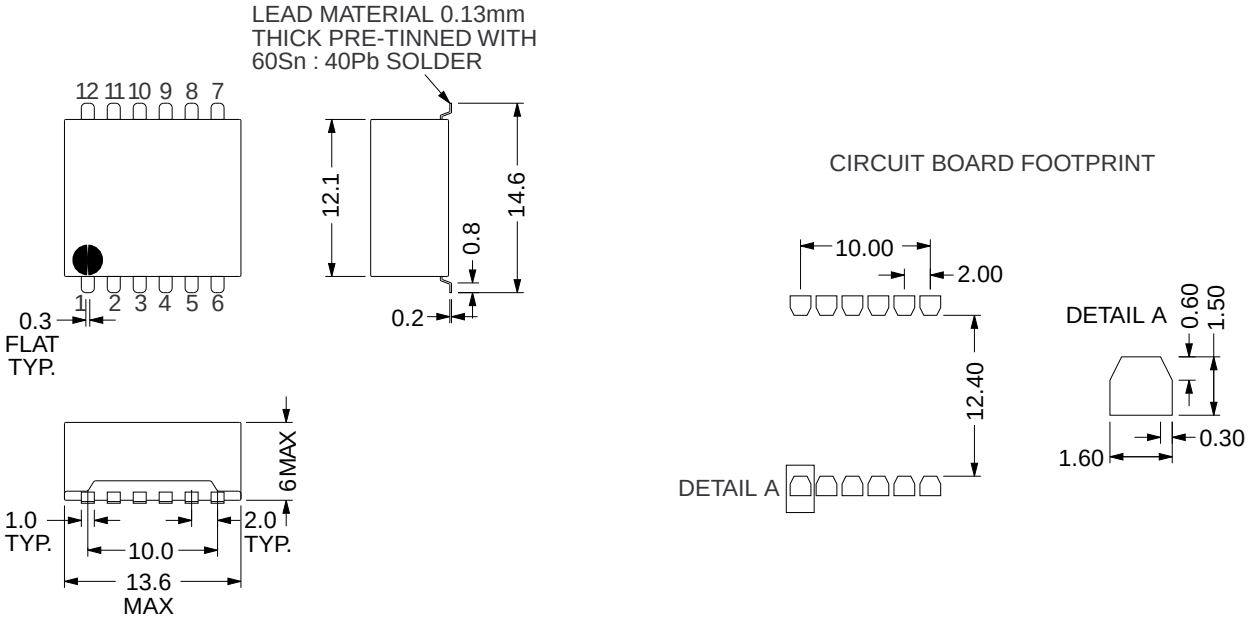
Package Dimensions



Environmental Specifications

Devices are designed to operate over the temperature range of -30°C to +70°C and after exposure to the shock, vibration, thermal shock and moisture conditions typically encountered in base station and subscriber terminal environments.

Functional Configuration

Lead	Configuration	Lead	Configuration
1	Ground	7	Ground
2	Clock Input	8	Reference Frequency Input
3	V_{CC1} (VCO)	9	V_{CC2} (PLL)
4	Lock Detector Output	10	Data Input
5	RF Output	11	Strobe Input
6	Ground	12	Ground

Absolute Maximum Ratings[1, 3]

Parameter	Absolute Maximum
Supply Voltage (V_{CC1})[2]	+6.5V
Supply Voltage (V_{CC2})[2]	+6.5V
Reference Frequency Voltage	-0.3V to +6.5V
Data, Clock, Strobe Voltages	-0.3V to +6.5V
Storage Temperature	-40°C to +80°C
Solder Assembly Temperature	220°C max for 10s

1. Exceeding these limits may cause permanent damage.
2. A series resistor will allow operation at any greater supply voltage. Used in conjunction with a bypass capacitor this will yield improved power supply decoupling and noise suppression.
3. Static sensitive, observe appropriate precautions.

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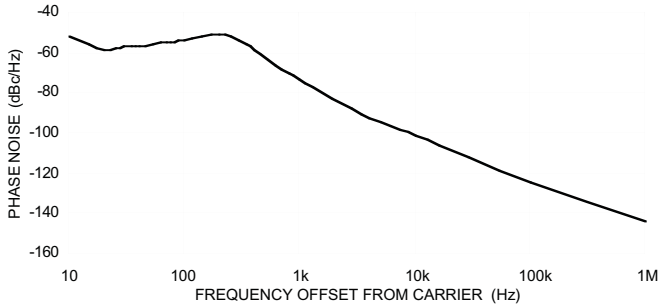
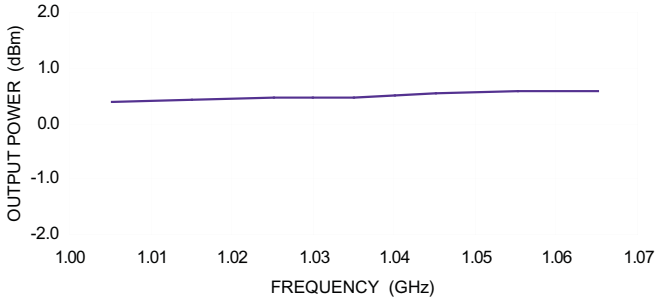
Typical Performance @ +25°C

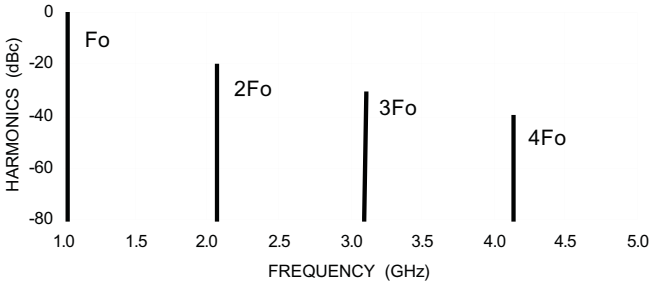
PHASE NOISE



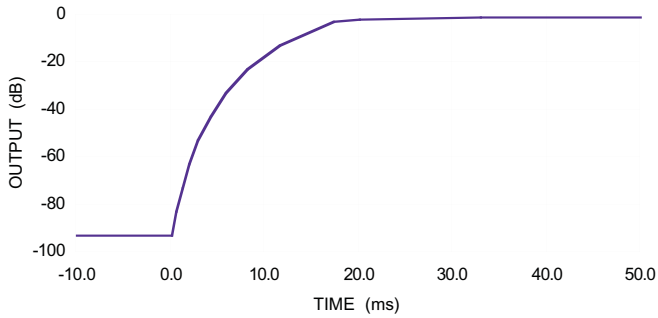
OUTPUT POWER



HARMONICS



SWITCHING SPEED



Measured using HP8561E Spectrum Analyser RBW 1 kHz, VBW 1 kHz, Span 0 Hz, Swp 50 ms.

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Programming Information

The output frequency of the synthesizer is serially programmed using the data input by sending a 16 bit reference word and a 19 bit frequency word with the clock input. Each word is followed by a strobe input pulse which must occur while the clock input is low. The data input timing is shown below.

The 16 bit reference word sends the prescalar range (S) (S = 0 for the prescalar range of 128 used), the reference division ratio (R) as a 14 bit binary number and a control bit. The 19 bit frequency word sends the number of prescalar division cycles (M) as an 11 bit binary number, the number of P + 1 divisions (A) as a 7 bit binary number and a control bit. Where:

$$R = \frac{F_R}{\Delta F}$$

$$M = \text{Integer of } \left(\frac{F_{out}}{\Delta F}\right) x \frac{1}{128}$$

$$A = \left[\left(\frac{F_{out}}{\Delta F}\right) x \frac{1}{128} - M\right] x 128$$

and R, M and A are all integers with $M \geq A$.

The output frequency is then determined by the following formula:

$$F_{out} = \left[(128 x M) + A\right] x \frac{F_R}{R}$$

For example with a 19.2 MHz reference frequency, to set the output frequency to 1035 MHz with a 12.5 kHz step size the following data words are required.

Prescalar range = 128, therefore S = 0

$$R = \frac{F_R}{\Delta F} = \frac{19.2 \text{ x } 10^6}{12.5 \text{ x } 10^3} = 1536 = 11000000000 \text{ binary}$$

Therefore the reference word is

0	00011000000000	1
S	R13 .....R0	Control bit

M = Integer of

$$\left(\frac{1035 \text{ x } 10^6}{12.5 \text{ x } 10^3}\right) x \ \frac{1}{128} = 646 = 1010000110 \text{ binary}$$

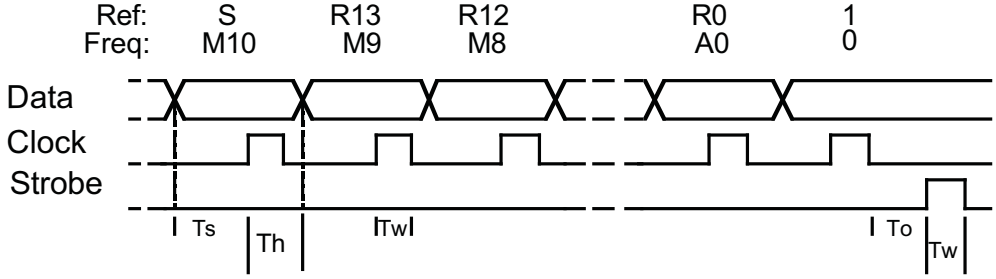
$$A = \left[\left(\frac{1035 \text{ x } 10^6}{12.5 \text{ x } 10^3}\right) x \frac{1}{128} - 646\right] \text{ x } 128 = 112 = 1110000 \text{ binary}$$

Therefore the frequency word is

01010000110	1110000	0
M10 ..... M0	A6.....A0	Control bit

Once the reference word has been sent, only the 19 bit frequency word need be sent to change the output frequency if the reference and step size remain constant.

Timing Diagram



Set-up time (Ts), Hold time (Th), Clock and Strobe pulsewidths (Tw) and Strobe offset time (To) all to be greater than 100 nanosec.

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